Amendments to the Claims:

Please withdraw from consideration claims 72 and 81-86 as follows.

Please amend claims 54, 65, 66, 77, 78, 79, 80, 87, 91, 93, 106, 110 and 112 as follows.

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. - 53. (Canceled)

54. (Currently Amended) A memory system having a stub configuration comprising:

a controller for generating a first clock signal, a control signal, an address signal and data signals on a data bus, the data bus, first clock signal, control signal, and address signal being arranged on a system bus in a stub configuration;

a memory module including memory devices coupled to the controller via the system bus;

a second clock signal generator independent of both the controller and the memory module for generating a second clock signal independently from the first clock signal that is sourced at a location that is beyond an outermost memory module on the system bus relative to the controller, the memory module receiving the first clock signal, the second clock signal and the control signal that includes a read or write command;

the first clock signal propagating from the controller to the memory module in a first direction of propagation, and the second clock signal propagating from the memory module to the controller in a second direction of propagation;

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal; and

the memory module, in response to the read command, initiating a read operation for reading data from the memory to the data bus in response to the second clock signal, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.

55. (Original) The memory system of claim 54 wherein the first clock signal comprises a write clock and wherein the second clock signal comprises a read clock.

56. (Original) The memory system of claim 55 wherein the memory controller further compensates for phase difference between the received second clock signal and the data signals on the data bus.

57. - 64. (Cancelled)

65. (Currently Amended) A method of transferring data in a memory system having a stub configuration comprising:

generating a first clock signal, a control signal, an address signal and data signals on a data bus at a controller, the data bus, first clock signal, control signal, and address signal being arranged on a system bus in a stub configuration;

generating a second clock signal independently from the first clock signal at a second clock signal generator independent of both the controller and a memory module including memory devices coupled to the controller via the system bus such that the second clock signal is sourced at a location that is beyond an outermost memory module on the system bus relative to the controller;

receiving the first clock signal, the second clock signal and the control signal that includes a read or write command at the memory module;

transmitting the first clock signal from the controller to the memory module in a first direction of propagation, and transmitting the second clock signal from the memory module to the controller in a second direction of propagation;

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal; and

the memory module, in response to the read command, initiating a read operation for reading data from the memory to the data bus in response to the

second clock signal, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.

66. (Currently Amended) A memory system having a stub configuration comprising:

a controller for generating a first clock signal, a control signal, an address signal and data signals on a first clock signal line, a control signal line, an address signal line and a data bus, respectively; and

a first memory module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal;

the first memory module, in response to a write command, initiating a write operation for writing the data signals from the data bus to the at least one memory device in synchronization with the first clock signal; and

the first memory module, in response to a read command, initiating a read operation for reading data from the at least one memory device to the data bus, and the control/address buffer device generating a second clock signal in response to the first clock signal, the second clock signal being provided to the controller on a second clock signal line that is separate from the first clock signal line, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.

67. (Previously Presented) The memory system of claim 66 wherein the memory system further includes a second memory module, the first and second memory modules generating respective first and second independent return clock signals as the second clock signal, and further comprising a motherboard coupling the first and second memory modules and the controller, the motherboard including the data bus, the control signal line, the address signal line, the first clock signal line and first and second independent

return clock signal lines for transfer of the first and second return clock signals from the first and second memory modules to the controller.

68. (Previously Presented) The memory system of claim 67 wherein the first and second return clock signal lines are crossed on the motherboard between the first and second memory modules.

69. (Previously Presented) The memory system of claim 67 wherein the first return clock signal line is coupled to a dummy load on the second memory module and wherein the second return clock signal line is coupled to a dummy load on the first memory module.

70. (Previously Presented) The memory system of claim 69 wherein the dummy load comprises a load capacitor or a dummy pin.

71. (Previously Presented) The memory system of claim 69 wherein the dummy load is selected to match the capacitance loading of the data bus.

72. (Withdrawn) The memory system of claim 66 wherein the control/address buffer further receives a first flag signal from the controller and provides a second flag signal to the controller during the read operation, the controller receiving the read data from the at least one memory device in response to the second clock signal and the second flag signal.

73. (Previously Presented) The memory system of claim 66 wherein the first clock signal comprises a write clock and wherein the second clock signal comprises a read clock.

74. (Previously Presented) The memory system of claim 66 wherein the system comprises multiple memory modules and wherein the multiple memory modules each generate independent second clock signals, the second clock signals each being different in phase relative to each other.

75. (Previously Presented) The memory system of claim 74 wherein the phases of the multiple second clock signals are different in phase due to the difference in propagation delay between each of the memory modules and the controller.

76. (Previously Presented) The memory system of claim 66 wherein the propagation delay of the second clock signal on the second clock signal line from the first memory module to the controller is substantially equal to that of the data signals on the data bus.

77. (Currently Amended) The memory system of claim 66 wherein the control/address buffer device further includes a phase locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal.

78. (Currently Amended) The memory system of claim 66 wherein the control/address buffer device further includes a delay locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal.

79. (Currently Amended) The memory system of claim 66 wherein the control/address buffer device includes a return path that is coupled to the first clock signal line that receives the first clock signal for generating the second clock signal in response to the first clock signal that is transmitted on the second clock signal line.

80. (Currently Amended) The memory system of claim 79 wherein the control/address buffer device further includes a capacitor having a capacitance that is selected to compensate for capacitive loading on the data bus by the at least one memory device of the memory module; the capacitor being coupled to a junction of the first clock signal line and the return path.

81. (Withdrawn) The memory system of claim 66 further comprising a first flag signal generated by the controller, the first memory module, in response to the first flag signal, controlling timing of initiation of the write operation or read operation, and if a read operation is commanded, generating a second flag signal in response to the first flag

signal, the second flag signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second clock signal and the second flag signal during a read operation.

82. (Withdrawn) The memory system of claim 81 wherein the memory system further includes a second memory module, the first and second memory modules generating respective first and second independent second flag signals, and further comprising a motherboard coupling the first and second memory modules and the controller, the motherboard including the data bus, a control bus for transfer of the control signal, an address bus for transfer of the address signal; a first flag signal line for transfer of the first flag signal, and first and second independent return flag signal lines for transfer of the first and second return flag signals, the first flag signal line and the first and second return flag signal lines being routed with the control bus and the address bus.

83. (Withdrawn) The memory system of claim 82 wherein the first and second return flag signal lines are crossed on the motherboard between the first and second modules.

84. (Withdrawn) The memory system of claim 82 wherein the first return flag signal line is coupled to a dummy load on the second memory module and wherein the second return flag signal line is coupled to a dummy load on the first memory module.

85. (Withdrawn) The memory system of claim 84 wherein the dummy load comprises a load capacitor or a dummy pin.

86. (Withdrawn) The memory system of claim 84 wherein the dummy load is selected to match the capacitance loading of the data bus.

87. (Currently Amended) The memory system of claim 66 wherein the control/address buffer device is mounted to a first side of the first memory module, and further comprising a dummy load for coupling to a first signal line of the control/address buffer device to provide load matching with a load experienced by a second signal line of the memory devices mounted to both first and second sides of the memory module.

88. (Previously Presented) The memory system of claim 87 wherein the dummy load comprises a load capacitor or a dummy pin.

89. (Previously Presented) The memory system of claim 87 wherein the first signal line comprises the first clock signal line or the second clock signal line, and wherein the second signal line comprises the data bus or the first clock signal line.

90. (Previously Presented) The memory system of claim 66 wherein, during the read operation, the data signals and the second clock signal are output from the first memory module in synchronization with the first clock signal.

91. (Currently Amended) A memory system having a stub configuration, comprising:

a controller for generating a first clock signal, a control signal, an address signal and data signals on a first clock signal line, a control signal line, an address signal line and a data bus, respectively; and

a first memory module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal;

the first memory module, in response to a write command, initiating a write operation for writing the data signals from the data bus to the at least one memory device in synchronization with the first clock signal; and

the first memory module, in response to a read command, initiating a read operation for reading data from the at least one memory device to the data bus, and the clock return providing a second clock signal in response to the first clock signal, the second clock signal being provided to the controller on a second clock signal line that is separate from the first clock signal line, the controller receiving

the data signals on the data bus in response to the second clock signal during the read operation.

92. (Previously Presented) The memory system of claim 91 wherein the first memory module further includes a capacitor having a capacitance that is selected to compensate for capacitive loading on the data bus by the at least one memory device of the memory module; the capacitor being coupled to a junction of the first clock signal line and the clock return.

93. (Currently Amended) The memory system of claim 91 wherein the first memory module further includes a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal.

94. (Previously Presented) The memory system of claim 91 wherein the clock return comprises a phase locked loop coupled to the first clock signal line that receives the first clock signal and generates the second clock signal on the second clock signal line in response to the first clock signal.

95. (Previously Presented) The memory system of claim 91 wherein the clock return comprises a delay locked loop coupled to the first clock signal line that receives the first clock signal and generates the second clock signal on the second clock signal line in response to the first clock signal.

96. (Previously Presented) The memory system of claim 91 wherein the memory system further includes a second memory module, the first and second memory modules generating respective first and second independent return clock signals as the second clock signal, and further comprising a motherboard coupling the first and second memory modules and the controller, the motherboard including the data bus, the control signal line, the address signal line, the first clock signal line and first and second independent return clock signal lines for transfer of the first and second return clock signals from the first and second memory modules to the controller.

97. (Previously Presented) The memory system of claim 96 wherein the first and second return clock signal lines are crossed on the motherboard between the first and second memory modules.

98. (Previously Presented) The memory system of claim 96 wherein the first return clock signal line is coupled to a dummy load on the second memory module and wherein the second return clock signal line is coupled to a dummy load on the first memory module.

99. (Previously Presented) The memory system of claim 98 wherein the dummy load comprises a load capacitor or a dummy pin.

100. (Previously Presented) The memory system of claim 98 wherein the dummy load is selected to match the capacitance loading of the data bus.

101. (Previously Presented) The memory system of claim 91 wherein the first clock signal comprises a write clock and wherein the second clock signal comprises a read clock.

102. (Previously Presented) The memory system of claim 91 wherein the system comprises multiple memory modules and wherein the multiple memory modules each generate independent second clock signals, the second clock signals each being different in phase relative to each other.

103. (Previously Presented) The memory system of claim 102 wherein the phases of the multiple second clock signals are different in phase due to the difference in propagation delay between each of the memory modules and the controller.

104. (Previously Presented) The memory system of claim 91 wherein the propagation delay of the second clock signal on the second clock signal line from the first memory module to the controller is substantially equal to that of the data signals on the data bus.

105. (Previously Presented) The memory system of claim 91 wherein, during the read operation, the data signals and the second clock signal are output from the first memory module in synchronization with the first clock signal.

106. (Currently Amended) A method of transferring data in a memory system having a stub configuration comprising:

generating a first clock signal, a control signal, an address signal and data signals at a controller on a first clock signal line, a control signal line, an address signal line and a data bus, respectively; and

receiving the data signals and the first clock signal at a first memory module including at least one memory device connected to the data bus and the first clock signal line respectively, and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal at a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line respectively,

the first memory module, in response to a write command, initiating a write operation for writing the data signals from the data bus to the at least one memory device in synchronization with the first clock signal; and

the first memory module, in response to a read command, initiating a read operation for reading data from the at least one memory device to the data bus, and the control/address buffer device generating a second clock signal in response to the first clock signal, the second clock signal being provided to the controller on a second clock signal line that is separate from the first clock signal line, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.

107. (Previously Presented) The method of claim 106 wherein the memory system further includes a second memory module, the first and second memory modules generating respective first and second independent return clock signals as the second clock signal, and further comprising a motherboard coupling the first and second memory

modules and the controller, the motherboard including the data bus, the control signal line, the address signal line, the first clock signal line and first and second independent return clock signal lines for transfer of the first and second return clock signals from the first and second memory modules to the controller.

108. (Previously Presented) The method of claim 107 wherein the first and second return clock signal lines are crossed on the motherboard between the first and second memory modules.

109. (Previously Presented) The method of claim 107 wherein the first and second independent return clock signals are different in phase.

110. (Currently Amended) A method of transferring data in a memory system having a stub configuration comprising:

generating a first clock signal, a control signal, an address signal and data signals at a controller on a first clock signal line, a control signal line, an address signal line and a data bus, respectively; and

receiving the data signals and the first clock signal at a first memory module including at least one memory device connected to the data bus and the first clock signal line respectively, and receiving the first clock signal at a clock return that is coupled to the first clock signal line and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal, at a control/address buffer device,

the first memory module, in response to a write command, initiating a write operation for writing the data signals from the data bus to the at least one memory device in synchronization with the first clock signal; and

the first memory module, in response to a read command, initiating a read operation for reading data from the at least one memory device to the data bus, and the clock return providing a second clock signal in response to the first clock signal, the second clock signal being provided to the controller on a second clock signal line that is separate from the first clock signal line, the controller receiving

the data signals on the data bus in response to the second clock signal during the read operation.

111. (Previously Presented) The method of claim 110 wherein the first memory module further includes a capacitor having a capacitance that is selected to compensate for capacitive loading on the data bus by the at least one memory device of the memory module; the capacitor being coupled to a junction of the first clock signal line and the clock return.

112. (Currently Amended) The method of claim 110 wherein the first memory module further includes a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal.

113. (Previously Presented) The method of claim 110 wherein the clock return comprises a phase locked loop coupled to the first clock signal line that receives the first clock signal and generates the second clock signal on the second clock signal line in response to the first clock signal.

114. (Previously Presented) The method of claim 110 wherein the clock return comprises a delay locked loop coupled to the first clock signal line that receives the first clock signal and generates the second clock signal on the second clock signal line in response to the first clock signal.